Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

1. (Previously presented) An integrated circuit chip comprising:

a semiconductor substrate;

a transistor in and on said semiconductor substrate;

multiple metal and dielectric layers over said semiconductor substrate;

a first contact pad over said semiconductor substrate;

a second contact pad over said semiconductor substrate;

a passivation layer over said multiple metal and dielectric layers, wherein said passivation layer comprises a nitride, wherein a first opening in said passivation layer is over a first contact point of said first contact pad, and said first contact point is at a bottom of said first opening, and wherein a second opening in said passivation layer is over a second contact point of said second contact pad, and said second contact point is at a bottom of said second opening;

a power metal structure over said passivation layer and on said first contact point, wherein said power metal structure is connected to said first contact point through said first opening, wherein said power metal structure comprises a copper layer, wherein said power metal structure has a first region configured to be wirebonded thereto for connection made to a next level of packaging;

a ground metal structure over said passivation layer and on said second contact point, wherein said ground metal structure is connected to said second contact point through said second opening, wherein said ground metal structure comprises a copper layer, wherein said ground metal structure has a second region configured to be wirebonded thereto for connection made to said next level of packaging;

a capacitor over said passivation layer, vertically over said power and ground metal structures and vertically over said first contact point;

a first solder joint vertically over said first contact point and between a first terminal of said capacitor and said power metal structure, wherein said first solder joint connects said first terminal to said power metal structure; and

a second solder joint between a second terminal of said capacitor and said ground metal structure, wherein said second solder joint connects said second terminal to said ground metal structure.

Claims 2-3 (Cancelled)

4. (Withdrawn) The integrated circuit chip according to claim 1 further comprising a polymer layer on said passivation layer, wherein said power and ground metal structures are further on said polymer layer.

Claims 5-6 (Cancelled)

7. (Previously presented) The integrated circuit chip according to claim 1, wherein said ground metal structure further comprises a gold layer over said copper layer of said ground metal structure.

Claim 8 (Cancelled)

9. (Currently amended) An integrated circuit chip comprising:

a semiconductor substrate;

a transistor in and on said semiconductor substrate;

multiple metal and dielectric layers over said semiconductor substrate;

a first contact pad over said semiconductor substrate;

a passivation layer over said multiple metal and dielectric layers, wherein a first opening in said passivation layer is over a first contact point of said first contact pad, and said first contact point is at a bottom of said first opening, wherein said passivation layer comprises a nitride;

a second contact pad over said semiconductor substrate, wherein said second contact pad is connected to said first contact point through said first opening, wherein said second contact pad comprises a first ~~substantive~~ gold layer with a thickness greater than 1 micrometer;

a capacitor over said passivation layer and said second contact pad;

a solder joint between a terminal of said capacitor and said second contact pad, wherein said solder joint connects said terminal to said second contact pad; and

a third contact pad between said solder joint and said second contact pad, wherein said third contact pad comprises electroplated copper, wherein a contact area between said third contact pad and said second contact pad is not vertically over ~~horizontally offset from~~ said first contact point.

10. (Previously presented) The integrated circuit chip according to claim 9 further comprising a fourth contact pad over said semiconductor substrate, wherein a second opening in said passivation layer is over a second contact point of said fourth contact pad, and said second contact point is at a bottom of said second opening, wherein said second contact point is configured to be wirebonded thereto for connection made to a next level of packaging.

11. (Previously presented) The integrated circuit chip according to claim 9 further comprising a fourth contact pad over said passivation layer, wherein said fourth contact pad is configured to be wirebonded thereto for connection made to a next level of packaging.

12. (Previously presented) The integrated circuit chip according to claim 9 further comprising a fourth contact pad over said semiconductor substrate, wherein a second opening in said passivation layer is over a second contact point of said fourth contact pad, and said second contact point is at a bottom of said second opening, and a fifth contact pad on said second contact point, wherein said fifth contact pad is configured to be wirebonded thereto for connection made to a next level of packaging.

Claims 13-14 (Cancelled)

15. (Currently amended) An integrated circuit chip comprising:

a semiconductor substrate;

a transistor in and on said semiconductor substrate;

multiple metal and dielectric layers over said semiconductor substrate;

a first contact pad over said semiconductor substrate;

a passivation layer over said multiple metal and dielectric layers, wherein said passivation layer comprises a nitride, wherein a first opening in said passivation layer is over a first contact point of said first contact pad, and said first contact point is at a bottom of said first opening;

a second contact pad over said semiconductor substrate, wherein said second contact pad is connected to said first contact point through said first opening;

a third contact pad over said semiconductor substrate, wherein said third contact pad is connected to said first contact point through said first opening and connected to said second contact pad, wherein said third contact pad has a region that is configured to be wirebonded thereto for connection made to a next level of packaging and is ~~horizontally offset from~~ not vertically over said first contact point;

a first polymer layer over said passivation layer, wherein a second opening in said first polymer layer is over a second contact point of said second contact pad, and said second contact point is at a bottom of said second opening;

a capacitor over said first polymer layer and said second contact point; and

a solder joint between said second contact point and a terminal of said capacitor, wherein said solder joint connects said terminal to said second contact point.

Claim 16 (Cancelled)

17. (Previously presented) The integrated circuit chip according to claim 15, wherein said second contact pad comprises a gold layer.

18. (Previously presented) The integrated circuit chip according to claim 15, wherein said second contact pad comprises a copper layer.

19. (Previously presented) The integrated circuit chip according to claim 15, wherein a ground

voltage is applied to said first contact pad.

Claim 20 (Cancelled)

21. (Previously presented) The integrated circuit chip according to claim 15, wherein a power supply voltage is applied to said first contact pad.

22. (Previously presented) The integrated circuit chip according to claim 15, wherein said second contact point is further vertically over said passivation layer.

Claims 23-24 (Cancelled)

25. (Previously presented) The integrated circuit chip according to claim 15, wherein said nitride comprises silicon nitride.

Claim 26 (Cancelled)

27. (Previously presented) The integrated circuit chip according to claim 15, wherein said third contact pad comprises a gold layer.

Claim 28 (Cancelled)

29. (Withdrawn) The integrated circuit chip according to claim 15 further comprising a second polymer layer on said passivation layer, wherein said second and third contact pads and said first polymer layer are further on said second polymer layer.

30. (Withdrawn) The integrated circuit chip according to claim 29, wherein said second polymer layer comprises polyimide.

Claims 31-90 (Cancelled)

91. (Previously presented) The integrated circuit chip according to claim 1, wherein said nitride comprises silicon nitride.

Claims 92-95 (Cancelled)

96. (Previously presented) The integrated circuit chip according to claim 1, wherein said ground metal structure further comprises a nickel layer over said copper layer of said ground metal structure.

97. (Previously presented) The integrated circuit chip according to claim 1 further comprising a polymer layer on said power and ground metal structures, wherein a third opening in said polymer layer is over a third contact point of said power metal structure, and said third contact point is at a bottom of said third opening, and wherein a fourth opening in said polymer layer is over a fourth contact point of said ground metal structure, and said fourth contact point is at a bottom of said fourth opening, wherein said first solder joint is between said first terminal and said third contact point and connects said first terminal to said third contact point through said third opening, and said second solder joint is between said second terminal and said fourth contact point and connects said second terminal to said fourth contact point through said fourth opening.

98. (Previously presented) The integrated circuit chip according to claim 9, wherein said capacitor comprises a decoupling capacitor.

99. (Previously presented) The integrated circuit chip according to claim 9, wherein said nitride comprises silicon nitride.

Claim 100 (Cancelled)

101. (Previously presented) The integrated circuit chip according to claim 15, wherein said capacitor comprises a decoupling capacitor.

102. (Previously presented) The integrated circuit chip according to claim 15, wherein a third opening in said first polymer layer is over said region of said third contact pad, and said region is at a bottom of said third opening.

103. (Previously presented) The integrated circuit chip according to claim 15, wherein said first polymer layer comprises polyimide.

Claims 104-107 (Cancelled)

108. (Previously presented) The integrated circuit chip according to claim 15, wherein said first polymer layer has a thickness between 2 and 150 micrometers.

109. (Previously presented) The integrated circuit chip according to claim 15, wherein a ground voltage is applied to said first, second and third contact pads.

110. (Previously presented) The integrated circuit chip according to claim 15, wherein a power supply voltage is applied to said first, second and third contact pads.

111. (Previously presented) The integrated circuit chip according to claim 15, wherein said passivation layer further comprises an oxide.

112. (Previously presented) The integrated circuit chip according to claim 15, wherein said passivation layer further comprises silicon oxide.

113. (Previously presented) The integrated circuit chip according to claim 97, wherein said polymer layer comprises polyimide.

114. (Previously presented) The integrated circuit chip according to claim 97, wherein said polymer layer has a thickness between 2 and 150 micrometers.

115. (Withdrawn) The integrated circuit chip according to claim 4, wherein said polymer layer comprises polyimide.

116. (Previously presented) The integrated circuit chip according to claim 1, wherein said passivation layer further comprises an oxide.

117. (Previously presented) The integrated circuit chip according to claim 1, wherein said passivation layer further comprises silicon oxide.

118. (Currently amended) The integrated circuit chip according to claim 11, ~~12,~~ wherein said fourth contact pad comprises a second ~~substantive old~~ gold layer.

119. (Previously presented) The integrated circuit chip according to claim 9 further comprising a polymer layer over said passivation layer, wherein a second opening in said polymer layer is over a second contact point of said second contact pad, and said second contact point is at a bottom of said second opening, wherein said solder joint is between said terminal and said second contact point and connects said terminal to said second contact point through said second opening, wherein said third contact pad is between said solder joint and said second contact point.

120. (Previously presented) The integrated circuit chip according to claim 119, wherein said polymer layer has a thickness between 2 and 150 micrometers.

121. (Previously presented) The integrated circuit chip according to claim 9, wherein said passivation layer further comprises an oxide.

122. (Previously presented) The integrated circuit chip according to claim 9, wherein said passivation layer further comprises silicon oxide.

123. (Previously presented) The integrated circuit chip according to claim 1 further comprising a polymer layer on said power and ground metal structures, wherein a third opening in said

polymer layer is over said first region, and said first region is at a bottom of said third opening, and wherein a fourth opening in said polymer layer is over said second region, and said second region is at a bottom of said fourth opening.

124. (Previously presented) The integrated circuit chip according to claim 123, wherein said polymer layer comprises polyimide.

125. (Previously presented) The integrated circuit chip according to claim 123, wherein said polymer layer has a thickness between 2 and 150 micrometers.

126. (Previously presented) The integrated circuit chip according to claim 1 further comprising a polymer layer on said power and ground metal structures, wherein a third opening in said polymer layer is over a third contact point of said power metal structure, and said third contact point is at a bottom of said third opening, wherein a fourth opening in said polymer layer is over a fourth contact point of said ground metal structure, and said fourth contact point is at a bottom of said fourth opening, wherein a fifth opening in said polymer layer is over said first region, and said first region is at a bottom of said fifth opening, and wherein a sixth opening in said polymer layer is over said second region, and said second region is at a bottom of said sixth opening, wherein said first solder joint is between said first terminal and said third contact point and connects said first terminal to said third contact point through said third opening, and said second solder joint is between said second terminal and said fourth contact point and connects said second terminal to said fourth contact point through said fourth opening.

127. (Previously presented) The integrated circuit chip according to claim 126, wherein said polymer layer comprises polyimide.

128. (Previously presented) The integrated circuit chip according to claim 126, wherein said polymer layer has a thickness between 2 and 150 micrometers.

129. (Currently amended) An integrated circuit chip comprising:

a semiconductor substrate;

a transistor in and on said semiconductor substrate;

multiple metal and dielectric layers over said semiconductor substrate;

a first contact pad over said semiconductor substrate;

a passivation layer over said multiple metal and dielectric layers, wherein a first opening in said passivation layer is over a first contact point of said first contact pad, and said first contact point is at a bottom of said first opening, wherein said passivation layer comprises a nitride;

a second contact pad over said semiconductor substrate, wherein said second contact pad is connected to said first contact point through said first opening, wherein said second contact pad comprises a first ~~substantive~~ gold layer with a thickness greater than 1 micrometer;

a capacitor over said passivation layer and said second contact pad;

a solder joint between a terminal of said capacitor and said second contact pad, wherein said solder joint connects said terminal to said second contact pad; and

a third contact pad between said solder joint and said second contact pad, wherein said third contact pad is finished with a solder wettable material comprising gold, wherein a contact area between said third contact pad and said second contact pad is not vertically over ~~horizontally offset from~~ said first contact point.

130. (Previously presented) The integrated circuit chip according to claim 129 further comprising a fourth contact pad over said semiconductor substrate, wherein a second opening in said passivation layer is over a second contact point of said fourth contact pad, and said second contact point is at a bottom of said second opening, wherein said second contact point is configured to be wirebonded thereto for connection made to a next level of packaging.

131. (Previously presented) The integrated circuit chip according to claim 129 further comprising a fourth contact pad over said passivation layer, wherein said fourth contact pad is configured to be wirebonded thereto for connection made to a next level of packaging.

132. (Previously presented) The integrated circuit chip according to claim 129 further comprising a fourth contact pad over said semiconductor substrate, wherein a second opening in said passivation layer is over a second contact point of said fourth contact pad, and said second

contact point is at a bottom of said second opening, and a fifth contact pad on said second contact point, wherein said fifth contact pad is configured to be wirebonded thereto for connection made to a next level of packaging.

133. (Currently amended) The integrated circuit chip according to claim 132, wherein said fifth contact pad comprises a second ~~substantive~~ gold layer.

134. (Previously presented) The integrated circuit chip according to claim 129, wherein said capacitor comprises a decoupling capacitor.

135. (Previously presented) The integrated circuit chip according to claim 129, wherein said nitride comprises silicon nitride.

136. (Previously presented) The integrated circuit chip according to claim 129 further comprising a polymer layer over said passivation layer, wherein a second opening in said polymer layer is over a second contact point of said second contact pad, and said second contact point is at a bottom of said second opening, wherein said solder joint is further between said terminal and said second contact point and connects said terminal to said second contact point through said second opening, wherein said third contact pad is further between said solder joint and said second contact point.

137. (Previously presented) The integrated circuit chip according to claim 136, wherein said polymer layer has a thickness between 2 and 150 micrometers.

138. (Previously presented) The integrated circuit chip according to claim 129, wherein said passivation layer further comprises an oxide.

139. (Previously presented) The integrated circuit chip according to claim 129, wherein said passivation layer further comprises silicon oxide.